Claim 5 stands rejected under 35 U.S.C. § 103(a) over Aiello and Official Notice by the Examiner.

Rejections

Claims 1-4, 6-14, and 23-26 have been rejected under 35 U.S.C. § 102(b) as anticipated by Aiello. *Examiner's Office Action* p. 2 (20 Nov. 2002). Claim 5 has been rejected under 35 U.S.C. § 103(a) over Aiello and Official Notice by the Examiner. *Id.* More specifically, these claims have been rejected in light of Figure 2a and the associated text of Aiello. *Id.*

Applicant points out that it expressly discussed Aiello in the "Description of Related Art Section" of its application, and that its invention provides express novelty over Aiello. Specifically, with respect to Aiello, Applicant stated:

> A different solution is disclosed in US 6127723 where an integrated device in emitter-switching configuration is disclosed comprising a high voltage bipolar transistor and a low voltage transistor and wherein the quenching element, a Zener diode, is formed in the base region or in the emitter region of the high voltage bipolar transistor. In this way the integrated device occupies a limited space in the semiconductor chip and a low resistance in series with the quenching element is assured so that the power dissipation at the quenching stage is reduced.
>
> However this solution presents the disadvantage of reducing the whole area of the high voltage bipolar transistor and of the low voltage transistor in order to form the quenching element. In the case wherein the Zener diode is formed in the emitter region of the high voltage transistor, besides the reduction of the whole area of the low voltage transistor a reduction of the efficiency of the high voltage transistor in the zone underlying the Zener diode is achieved.

Applicant's Application p. 2. Accordingly, Applicant devised an invention that provides advantages over the prior art structures of Aiello. One advantage provided by Applicant's invention is that it avoids "the quenching element .. formed in the base region or in the emitter region of the high voltage bipolar transistor... [and thus] the disadvantage of reducing the whole area of the high voltage bipolar transistor and of the low voltage transistor in order to form the quenching element. in that the structures of Applicant's invention." In light of the following, Applicant asserts that its existing claims are patentable over the art of record. Applicant has also herein added two dependent claims by amendment to make the novelty giving rise to this advantage yet more apparent to the Examiner.

Applicant's claim 1 recites "a *quenching element* of the first transistor, which discharges current therefrom when said second transistor is turned off, said quenching element being coupled with the base terminal of the first transistor and with the other not drivable terminal of the second transistor, said *quenching element having* at least one *Zener diode* made in *polysilicon, said* at least one *polysilicon* Zener *diode* being *formed* on the *second surface* of said chip and *comprising a polysilicon layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction.*

As noted above, Aiello shows "the quenching element .. formed in the base region or in the emitter region of the high voltage bipolar transistor." Consequently, as can be seen by reference to Figure 2a of Aiello and its supporting text, the quenching element of Aiello is formed in an epitaxial layer, or a layer of a *single crystal* semiconducting material grown on a host substrate which determines its orientation. A single crystal semiconducting material is not polysilicon. Thus, Aiello does not show or suggest at least the foregoing italicized portions of independent claim 1. Consequently, Aiello does not anticipate claim 1, and Applicant asks that Examiner hold claim 1 allowable over Aiello.

Applicant's claim 23 recites "*a zener diode formed in the polysilicon layer and including first and second junction regions having first and second types of conductivity, respectively, the diode being configured to discharge current from the first region when the second transistor is turned off.* Although the language of claim 23 differs from that of claim 1, the allowability of claim 23 will be apparent in view of the discussion of claim 1. As discussed above, Aiello does not show discuss at least the italicized the recitations of claim 23. Consequently, Aiello does not anticipate claim 23.

Claims 2-14 and 24-26 respectively depend either directly or indirectly from independent claims 1 and 23. Accordingly, the art of record does not anticipate such dependent claims for at least the reasons of such dependencies.

Overall, the cited reference(s) do not singly, or in any motivated combination and/or modification, teach or suggest the claimed features of the embodiments recited in independent claims 1, and 23, and thus such claims are allowable. Because the remaining claims depend from allowable independent claims, and also because they include additional limitations, such claims are likewise allowable. If the undersigned attorney has overlooked a relevant

teaching in any of the references, the Examiner is requested to point out specifically where such teaching may be found.

In light of the above amendments and remarks, Applicant respectfully submits that all pending claims are allowable. Applicant, therefore, respectfully requests that the Examiner reconsider this application and timely allow all pending claims. The Examiner is encouraged to contact Mr. Cook by telephone to discuss the above and any other distinctions between the claims and the applied references, if desired. If the Examiner notes any informalities in the claims, he is encouraged to contact Mr. Cook by telephone to expediently correct such informalities.

Patentability now established, the remainder of the factual assertions by the Examiner are rendered moot, and hence Applicant does not explicitly address such factual assertions herein. The fact that the moot factual assertions are not addressed should not be taken as an admission of any sort, and Applicant reserves the right to contest the statements in such moot factual assertions at a later time, should such become necessary.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made**." If a conflict arises between the clean copy and the attached "version with markings to show changes made," this statement constitutes public notice that Applicant respectfully requests that its intent is that the version with markings to show changes made be considered controlling.

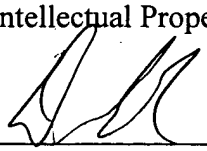
The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Sergio Tommaso Spampinato

SEED Intellectual Property Law Group PLLC



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend and/or add new claims as follows:

31. (New) The integrated device of claim 1 wherein said quenching element is on a first side of the second surface, and wherein substantially all semiconducting regions are on a second side of the second surface.

32. (New) The device of claim 23 further comprising:

the first, second, third, and fourth regions formed on a first side of the insulating layer; and

the polysilicon layer selectively formed on a second side of the insulating layer.

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